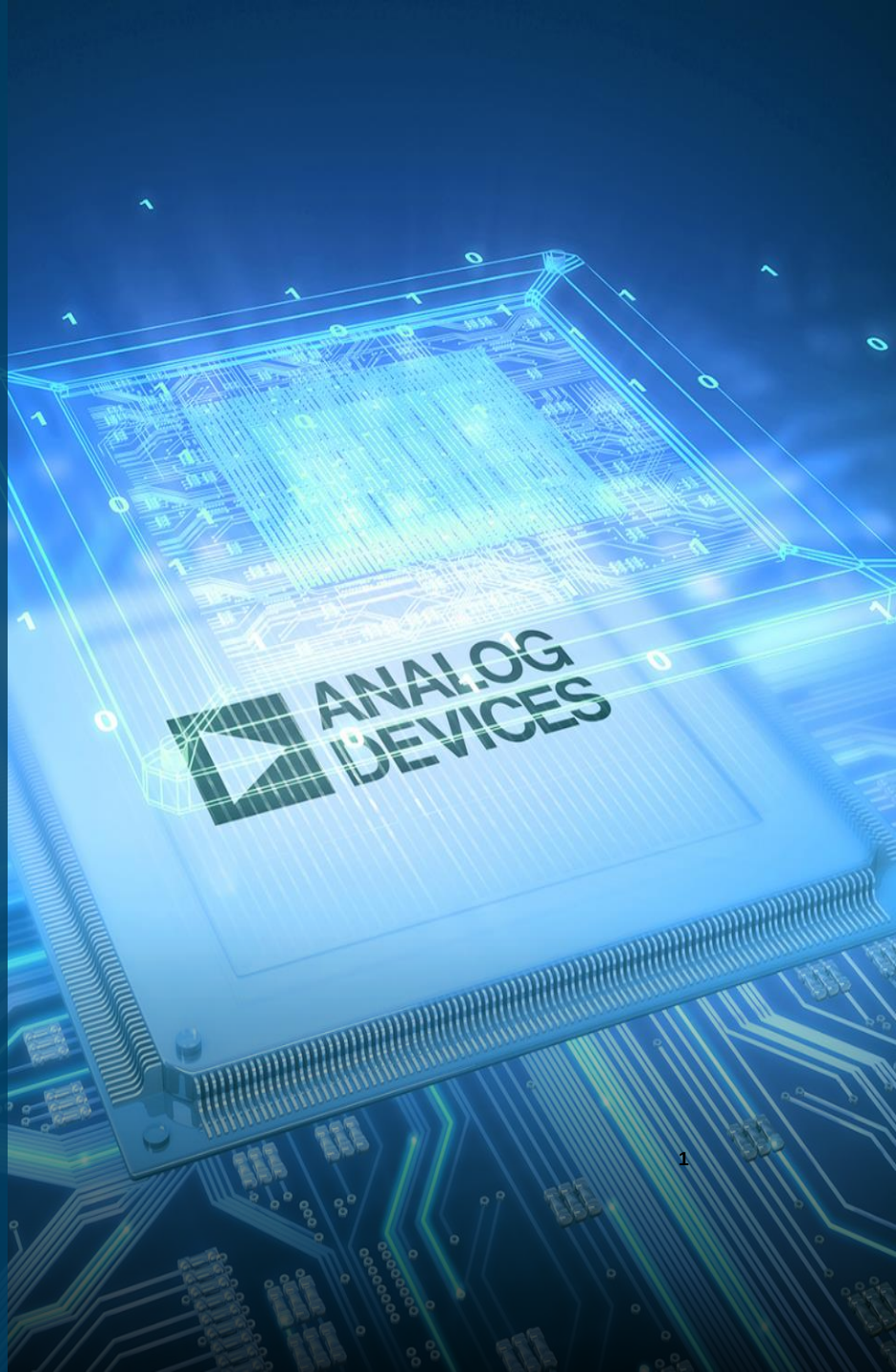
ANALOG DEVICES

AHEAD OF WHAT'S POSSIBLE™

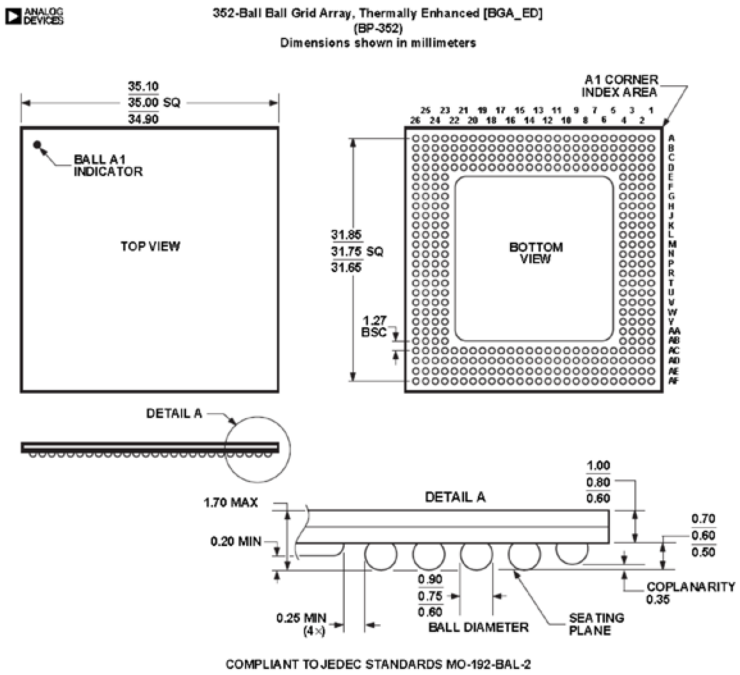
# ADN4605 Assembly Site Transfer and Data Sheet Revision_PCN

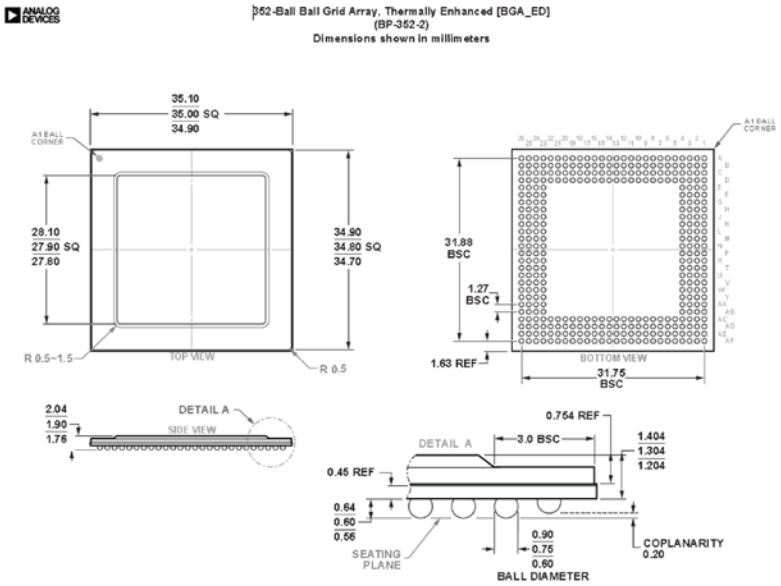





DATE: 07-27-2019

# Change #1- Package Outline Drawing




Current POD→ BP-352

1.7mm max height

New POD→ BP-352-2

2.04mm max height





ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

# Change #2 – Die Interconnect

- Current package uses wire bonded die
- New package uses flip chip die with solder bumps

# Change #3 Assembly Site

- New assembly site is STATS ChipPAC Korea




ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

# Change #4- Data Sheet Change

- Data sheet rev change from RevA to RevB.
- On page 2 under Revision History RevB changes were added.
- On page 4 Electrical Characteristics – Removed thermal characteristics section and note 2.
- On page 7 Absolute Maximum Ratings – Changed Internal Power Dissipation[1] rating from 8.4W to 11.5W
- On page 7 Absolute Maximum Ratings under NOTES1 – Change $\theta_{JA}$ = 9.2° C/W TO 8.5° C/W.
- On page 7 added Thermal Resistance Section.
- On page 55 Changed package outline drawing.
- On page 55 Ordering Guide – Changed package Option BP-352 to BP-352-2.

## ADN4605 Assembly Site Transfer and Data Sheet Revision

### Qualification Results Summary of ADN4605 BGA_ED
### Package Extension Qualification

| QUALIFICATION PLAN / STATUS | | | |
|---|---|---|---|
| **TEST** | **SPECIFICATION** | **SAMPLE SIZE** | **RESULTS** |
| Highly Accelerated Stress Test (HAST)* | JEDEC *JESD22-A110* | **3*32** | **Pass** |
| Temperature Cycle (TC)* | JEDEC *JESD22-A104* | **3*32** | **Pass** |
| High Temperature Storage Life (HTSL) | JEDEC *JESD22-A103* | **1*32** | **Pass** |
| Solder Heat Resistance (SHR)* | JEDEC/IPC *J-STD-020* | **3*11** | **Pass** |
| Electrostatic Discharge *Field-Induced Charged Device Model* | JEDEC *JS-002* | **3/voltage** | **Pass 500V** |

*Preconditioned per JEDEC/IPC J-STD-020